

THE CLAIMS

1. (Currently Amended) A data-empowered test program architecture stored on a computer readable storage medium, comprising:

a plurality of control files, each control file defining a test sequence for one of a plurality of units-under-test and instructions for executing the test sequence;

a test executive software module configured to select a test sequence in one of the plurality of control files to use based on a unit-under-test;

a test framework software module configured to receive a selected test sequence from the test executive software module, determine how to perform the selected test sequence, and perform the selected test sequence; and

a plurality of software components in a software components module coupled for interaction with the test framework software module and structured for outputting at least one test report.

2. (Original) The architecture of claim 1 wherein the test framework software module further comprises a hardware abstraction interface.

3. (Original) The architecture of claim 1, further comprising an external reuse library having one or more test descriptions of common signal types and being coupled for generating the control files.

4. (Original) The architecture of claim 1 wherein the software components module further comprises one or more software components for interfacing between the one or more external control files and one or more of the test executive software module and the test framework software module.

5. (Original) The architecture of claim 1 wherein the software components module further comprises a pass/fail analyzer and report generator having one or more modes of pass/fail analysis and test reporting.

6. (Previously Presented) A data-empowered test program architecture stored on a computer readable storage medium, comprising:

a plurality of external control files having a list of test identification numbers, each test identification number defining a test sequence and instructions for executing the test sequence;

a test executive module having an execution engine coupled to receive one or more test identification numbers from the list of test identification numbers based on a unit-under test, the test identification number configured to generate, as a function of the one or more test identification numbers, a plurality of test actions to be performed on the unit-under-test as defined in the test sequence;

a test framework module for accessing the plurality of test actions and the instructions, the test framework module configured to perform, based on the instructions, the steps of:

i) determining an identification of one of the test hardware resources associated with a current one of the test action,

ii) retrieving the identification of the associated test hardware resource,

iii) determining a signal type corresponding to the retrieved test hardware resource identification,

iv) accessing as a function of the signal type one of the external control files having test hardware resource card-type information, and

v) determining the test hardware resource card-type information as a function of a card-type identifier.

7. (Original) The architecture of claim 6 wherein the test hardware resource card-type information includes routing data and parameters for interfacing with an external hardware driver.

8. (Original) The architecture of claim 6, further comprising an external reuse library having a plurality of test descriptions corresponding to a plurality of different test signal types.
9. (Original) The architecture of claim 6, further comprising a plurality of software components for interfacing between the external control files and one or more of the test executive module and the test framework module.
10. (Original) The architecture of claim 9 wherein the plurality of software components further comprises one or more modes of pass/fail analysis and test reporting.
11. (Previously Presented) A computing device, comprising:
 - means for storing a plurality of test actions;
 - means for determining which test actions of the plurality of test actions are to be performed on one of a plurality of units-under-test;
 - means for determining which instructions to use when performing the plurality of test actions;
 - means for accessing the instructions;
 - means for identifying, based on the instructions, test hardware resources associated with a current one of the plurality of test actions; and
 - means for interfacing with an external hardware driver as a function of identifying the test hardware resources associated with the current one of the plurality of test actions.

12. (Previously Presented) The computing device of claim 11 wherein the means for interfacing with an external hardware driver further comprises:

- means for determining a signal type corresponding to the identified test hardware resource;
- means for accessing as a function of the signal type an external control file having test hardware resource card-type information contained therein; and
- means for determining the test hardware resource card-type information as a function of a card-type identifier.

13. (Previously Presented) The computing device of claim 11 wherein the means for generating a plurality of test actions further comprises means for generating the plurality of test actions as a function of one or more test identification numbers received from a list of test identification numbers.

14. (Previously Presented) The computing device of claim 11 wherein the means for generating a plurality of test actions to be performed on a unit-under-test further comprises means for generating a plurality of control files for configuring software code for generating the plurality of test actions.

15. (Previously Presented) The computing device of claim 14 wherein the means for generating a plurality of control files further comprises means for generating one or more of the control files as a function of one or more test descriptions of signal types contained in an external reuse library.

16. (Previously Presented) The computing device of claim 11, further comprising means for performing pass/fail analysis.

17. (Previously Presented) The computing device of claim 16, further comprising means for generating one or more test reports.

18. (Previously Presented) A computer-readable medium having instructions stored thereon, which instructions, when executed by a processor cause the processor to:

determine which test actions of a plurality of test actions to perform, the test action based on one of a plurality of units-under-test;

determine how to perform the test actions of the plurality of test actions based on the instructions;

perform the plurality of test actions based on the instructions;

identify a test hardware resource associated with a current one of the plurality of test actions; and

interface with an external hardware driver as a function of the test hardware resources associated with the current one of the plurality of test actions.

19. (Previously Presented) The computer-readable medium of claim 18 further comprising instructions which cause the processor to:

determine a signal type corresponding to the identified test hardware resource;

as a function of the signal type, access an external control file having test hardware resource card-type information contained therein; and

as a function of a card-type identifier, determine the test hardware resource card-type information.

20. (Previously Presented) The computer-readable medium of claim 18 further comprising instructions which cause the processor to:
- receive from a list of test identification numbers one or more test identification numbers, and
generate the plurality of test actions as a function of the received test identification number.
21. (Previously Presented) The computer-readable medium of claim 18, further comprising instructions which cause the processor to perform a pass/fail analysis.
22. (Previously Presented) The computer-readable medium of claim 21, further comprising instructions which cause the processor to generate one or more test reports.
23. (Previously Presented) The computer-readable medium of claim 18, further comprising instructions which cause the processor to:
- generate a plurality of test actions; and
access the plurality of the test actions.